REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated November 2, 2006 has been received and its contents carefully reviewed.

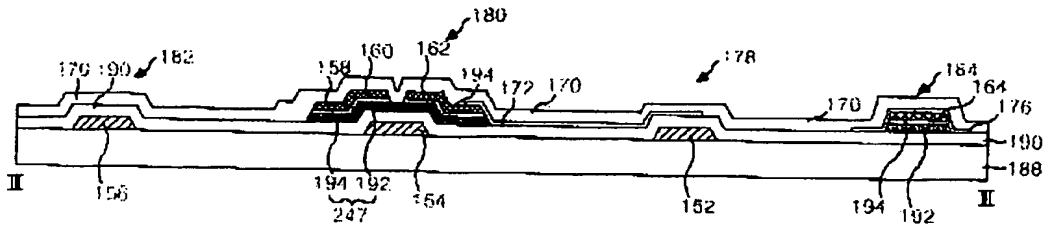
Claims 1, 5 and 6 are hereby amended. Accordingly, claims 1-3 and 5-6 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

In the Office Action, claims 1, 2 and 5-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,380,559 to Park et al. (hereinafter "Park") in view of U.S. Patent No. 6,429.057 to Hong et al. (hereinafter "Hong"). Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Hong and further in view of U.S. Patent No. 6,255,130 to Kim (hereinafter "Kim").

The rejection of claims 1, 2 and 5-6 are respectfully traversed and reconsideration is requested. Claims 1, 2 and 5-6 are allowable over the cited references in that each of the claims recites a combination of elements including, for example, "arranging a cutting-off plate on a remainder region of the substrate other than the region of the pad part" and "exposing the gate pad of the pad part and the data pad protection electrode by a etching process using the cutting-off plate, wherein the cutting-off plate is capable of being etched along with the protective film in the etching process." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. In particular, applicants submit that the structure of the claimed invention is different from that of Park in that Park merely discloses a mask that is used to expose light to form a photoresist pattern on a passivation layer (see abstract).

Applicants respectfully submit that a thin film transistor array substrate of the claimed invention is formed by use of 3-mask processes (see Fig. 10D).

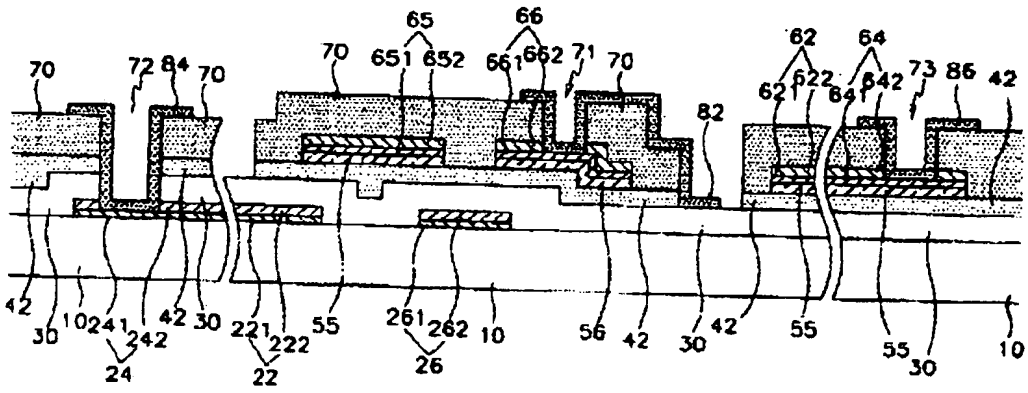
- Fig 10D -



That is, the claimed invention recites a combination of elements including, for example, forming a gate pattern including a gate electrode of the thin film transistor, the gate line connected to the gate electrode and the gate pad connected to the gate line on the substrate by use of a first masking process; forming a gate insulation film on the substrate where the gate pattern is formed; forming a source electrode and a drain electrode of the thin film transistor, a data line connected to the source electrode, a data pad connected to the data line, a source/drain pattern including a storage electrode in a region overlapped with the gate line, a semiconductor pattern formed in the lower part according to the source/drain pattern on the gate insulation film by use of a second masking process; forming a transparent electrode pattern including a pixel electrode and a data pad protection electrode by use of a third masking process, the pixel electrode is directly connected to the drain electrode and the storage electrode, and the data pad protection electrode is formed for covering the data pad; and forming entirely a protection film on the substrate without necessitating the use of a masking process.

On the contrary, a thin film transistor array substrate of Park is formed by use a 4-mask processes (see Fig. 4).

FIG.4



That is, Park discloses processes forming a gate pattern including a gate electrode, a gate line and a gate pad by use of a first masking process; forming a gate insulation film on the substrate; forming a source electrode, a drain electrode, a data line, a data pad, a semiconductor pattern by use of a second masking process; forming a passivation layer having a contact window by use of a third masking process [col. 2, line 59 - col. 3, line 13]; and forming a transparent electrode pattern including a pixel electrode and a data pad protection electrode by use of a fourth masking process.

Accordingly, Applicant respectfully submits that claim 1, and claims 2 and 5-6 which depend from claim 1, are allowable over the cited references. Additionally, claim 3 is allowable at least in virtue of the fact that it depends from claim 1.

Applicants believe the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps

necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: February 1, 2007

Respectfully submitted,

By _____

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